pointer information. Lai teaches a method to read data stored in the random access memory based on the contents of the read offset register. However, Lai teaches a network interface device that is only capable of reading and writing data as directed by a host CPU, separate from the network interface device, "[i]n the present invention, a receive byte offset register is used that enables the host CPU to begin reading a data frame from the SRAM memory 18 starting from any particular byte, as well as change the starting byte," [Lai, col. 6, lines 50-54]. Lai does not teach a network interface device that generates an output stream of data by executing a series of program instructions on data stored within a first-in-first-out buffer. The device taught by Lai only acts as a flexible buffer wherein the data in the buffer may be accessed in any order by the host CPU.

Lai describes using a first-in first-out buffer in a network interface device for storing transmit and receive data. [Lai, col. 1, lines 23-29] *However, Lai does not teach executing a series of program instructions or performing operations on the data stored within the first-in first-out buffer.* Lai does not teach or claim a device that can generate an output stream of data by executing a series of program instructions on a stored stream of data. *Lai also does not teach executing a series of program instructions and performing the operations on the stream of data stored in a first-in first-out buffer.*

Lai specifically teaches away from using a first-in first-out buffer in the network interface device. Further, Lai specifically teaches that

> [t]here is a need for an arrangement that enables the use of a random access memory in a network interface device, **as opposed to a FIFO buffer**, to store a data frame and to provide flexibility in reading the data frame. [Lai, col. 1, lines 48-52, emphasis added]

Lai teaches a memory unit that includes a **SRAM** which is accessed in a random access manner. [Lai, col. 3, lines 5-12] As described above, Lai also teaches a receive byte offset register that is used to enable the host CPU to begin reading a data frame from the **SRAM memory** starting from any particular byte. [Lai, col. 6, lines 50-54] The invention taught by Lai is not directed to reading out data in a first-in first-out manner, but rather reading out data starting at any location in the **SRAM memory**. As specifically taught by Lai,

> [t]his use of a read byte offset register 72 in connection with RB_MMU 22c provides the present invention with improved flexibility in reading data frames, as opposed to the use of a conventional *FIFO* which *requires* the data to be read out in a *first in, first out order*. [Lai, col. 7, lines 47-51, emphasis added]

Accordingly, Lai specifically teaches away from using a first-in first-out buffer.

Further, no where in Lai is it taught that a series of program instructions is performed on the data stored within the memory. Lai only teaches changing the starting location from which data is read. Lai does not teach performing a series of program instructions on the data itself. Lai also does not teach generating an output stream of data by executing the series of program instructions and performing the operations on the stored stream of data.

In contrast to the teachings of Lai, the programmable *first-in first-out buffer* of the present invention receives a stream of data to be buffered within the *first-in first-out buffer* and then output from the *first-in first-out buffer*. The programmable *first-in first-out buffer* includes the ability to receive *program instructions* from an application or control circuit to perform *specific operations on the stream of data* before the data is provided as an output from the programmable *first-in first-out buffer*. By performing the specific operations of the program instructions on the stored data, the programmable *first-in first-out buffer* has the ability to filter the stream of data as it passes through the *first-in first-out buffer*, including re-ordering data within the *first-in first-out buffer*, if appropriate, and also to synchronize the input and output of the stream of data with external input and output signals, respectively. As discussed above, Lai does not teach using a *first-in first-out buffer*. Further, Lai does not teach *executing a series of program instructions* and performing the operations on the stream of data stored in a *first-in first-out buffer*.

The independent Claim 1 is directed to a method of buffering data within a first-in first-out buffer. The method of Claim 1 comprises receiving a stream of data to be buffered within the *first-in first-out buffer*, storing the stream of data within the *first-in first-out buffer* thereby forming a stored stream of data, obtaining a series of program instructions specifying operations to be performed on the stored stream of data and generating an output stream of data by *executing the series of program instructions* and performing the operations on the stored stream of data. As discussed above, Lai teaches away from using a first-in first out buffer. Further, Lai does not teach obtaining a series of program instructions specifying operations to be performed on the stored stream of data in the first-in first-out buffer. Lai also does not teach generating an output stream of data by *executing the series of program instructions* and performing the operations on the stored stream of data in the *first-in first-out buffer*. For at least these reasons, the independent Claim 1 is allowable over the teachings of Lai.

Claims 2-4, 6, and 7 are dependent on the independent Claim 1. As described above, the independent Claim 1 is allowable over the teachings of Lai. Accordingly, Claims 2-4, 6, and 7 are all also allowable as being dependent on an allowable claim.

The independent Claim 9 is directed to a method of buffering data within a first-in first-out buffer. The method of Claim 9 comprises receiving a stream of data to be buffered within the *first-in first-out buffer*, storing the stream of data within the *first-in first-out buffer* thereby forming a stored stream of data, obtaining a series of program instructions specifying operations to be performed in relation to the stored stream of data and generating an output stream of data by *executing the series of program instructions* and performing the operations in relation to the stored stream of data, including synchronizing the output stream of data to a time reference. As discussed above, Lai teaches away from using a first-in first-out buffer. Further, Lai does not teach obtaining a series of program instructions specifying operations to be performed in relation to the stored stream of data in the first-in first-out buffer. Lai also does not teach generating an output stream of data by *executing the series of program instructions* and performing the operations in relation to the stored stream of data in the *first-in first-out buffer*. For at least these reasons, the independent Claim 9 is allowable over the teachings of Lai.

Claims 10-12, 14 and 15 are dependent on the independent Claim 9. As described above, the independent Claim 9 is allowable over the teachings of Lai. Accordingly, Claims 10-12, 14 and 15 are all also allowable as being dependent on an allowable claim.

The independent Claim 17 is directed to an apparatus for buffering data within a first-in first-out buffer. The apparatus of Claim 17 comprises means for receiving a stream of data to be buffered within the *first-in first-out buffer*, means for storing the stream of data within the *first-in first-out buffer* thereby forming a stored stream of data, means for obtaining a series of program instructions specifying operations to be performed on the stored stream of data and means for generating an output stream of data by *executing the series of program instructions* and performing the operations on the stored stream of data. As discussed above, Lai teaches away from using a first-in first-out buffer. Further, Lai does not teach a means for obtaining a series of program instructions specifying operations to be performed on the stored stream of data in the first-in first-out buffer. Lai also does not teach a means for generating an output stream of data by *executing the series of program instructions* and performing the operations on the stored stream of data in the *first-in first-out buffer*. For at least these reasons, the independent Claim 17 is allowable over the teachings of Lai.

Claims 18-20, 22, and 23 are dependent on the independent Claim 17. As described above, the independent Claim 17 is allowable over the teachings of Lai. Accordingly, Claims 18-20, 22, and 23 are all also allowable as being dependent on an allowable claim.

The independent Claim 25 is directed to a programmable first-in first-out buffer. The programmable first-in first-out buffer of Claim 25 comprises an input interface circuit configured

to receive a stream of data to be buffered within the *first-in first-out buffer*, a data memory coupled to the input interface circuit to store the stream of data, thereby forming a stored stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate an output stream of data by *executing the series of program instructions* and perform the operations on the stored stream of data. As discussed above, Lai teaches away from using a first-in first-out buffer. Further, Lai does not teach a program memory within a first-in first-out buffer configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data in the first-in first-out buffer. Lai also does not teach an execution unit coupled to the program memory and to the data memory to generate an output stream of data by *executing the series of program instructions* and perform the operations on the stored stream of data in the *first-in first-out buffer*. For at least these reasons, the independent Claim 25 is allowable over the teachings of Lai.

Claims 26-28, 30, and 31 are dependent on the independent Claim 25. As described above, the independent Claim 25 is allowable over the teachings of Lai. Accordingly, Claims 26-28, 30, and 31 are all also allowable as being dependent on an allowable claim.

The independent Claim 33 is directed to a system comprising a bus interface circuit configured to couple to a bus structure and receive a stream of data, a data memory coupled to the bus interface circuit to store the stream of data, thereby forming a stored stream of data, wherein the data memory stores and outputs the stored stream of data, thereby forming an output stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate the output stream of data by executing the series of program instructions and performing the operations on the stored stream of data. As discussed above, Lai does not teach a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data. Lai also does not teach an execution unit coupled to the program memory and to the data memory to generate the output stream of data by *executing the series of program instructions* and performing the operations on the stored stream of data. For at least these reasons, the independent Claim 33 is allowable over the teachings of Lai.

Claims 34, 35, 37, and 38 are dependent on the independent Claim 33. As described above, the independent Claim 33 is allowable over the teachings of Lai. Accordingly, Claims 34, 35, 37, and 38 are all also allowable as being dependent on an allowable claim.

The independent Claim 40 is directed to a network of devices. The network of devices of Claim 40 comprises a plurality of devices, a bus structure coupled between the plurality of devices to transmit data between the devices and a programmable *first-in first-out buffer* including an input interface circuit configured to receive a stream of data to be buffered within the *first-in first-out buffer*, a data memory coupled to the input interface circuit to store the stream of data, thereby forming a stored stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate the output stream of data by *executing the series of program instructions* and performing the operations on the stored stream of data. As discussed above, Lai teaches away from using a first-in first-out buffer. Further, Lai does not teach a program memory within a first-in first-out buffer configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data in the first-in first-out buffer. Lai also does not teach an execution unit coupled to the program memory and to the data memory to generate an output stream of data by *executing the series of program instructions* and perform the operations on the stored stream of data in the *first-in first-out buffer*. For at least these reasons, the independent Claim 40 is allowable over the teachings of Lai.

Claims 41, 42, 44, and 45 are dependent on the independent Claim 40. As described above, the independent Claim 40 is allowable over the teachings of Lai. Accordingly, Claims 41, 42, 44, and 45 are all also allowable as being dependent on an allowable claim.

Rejections under 35 U.S.C. §103

Within the Office Action, Claims 5, 8, 13, 16, 21, 24, 29, 32, 36, 39, 43 and 46 have been rejected under 35 U.S.C. §103(a) as being obvious over Lai. The applicant respectfully disagrees with this rejection.

Claims 5 and 8 are dependent upon the independent Claim 1. As discussed above, Claim 1 is allowable over the teachings of Lai. Accordingly, Claims 5 and 8 are both also allowable as being dependent upon an allowable base claim.

Claims 13 and 16 are dependent upon the independent Claim 9. As discussed above, Claim 9 is allowable over the teachings of Lai. Accordingly, Claims 14 and 16 are both also allowable as being dependent upon an allowable base claim.

Claims 21 and 24 are dependent upon the independent Claim 17. As discussed above, Claim 17 is allowable over the teachings of Lai. Accordingly, Claims 21 and 24 are both also allowable as being dependent upon an allowable base claim.

Claims 29 and 32 are dependent upon the independent Claim 25. As discussed above, Claim 25 is allowable over the teachings of Lai. Accordingly, Claims 29 and 32 are both also allowable as being dependent upon an allowable base claim.

Claims 36 and 39 are dependent upon the independent Claim 33. As discussed above, Claim 33 is allowable over the teachings of Lai. Accordingly, Claims 36 and 39 are both also allowable as being dependent upon an allowable base claim.

Claims 43 and 46 are dependent upon the independent Claim 40. As discussed above, Claim 40 is allowable over the teachings of Lai. Accordingly, Claims 43 and 46 are both also allowable as being dependent upon an allowable base claim.

For the reasons given above, the applicant respectfully submits that Claims 1-46 are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: January 13, 2004 By: Jonathan O. Owens

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CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

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